EGRE 426 Lab 4

Due Wednesday September 30, 2009

For this lab you may work in groups of two. A formal lab report is not necessary, but each group must email all source code to jhtucker@vcu.edu as an attachment no later than 3:30 p.m. next Monday. In the email, use as subject "EGRE 426 Lab 4 ALU your names". During the Monday Lab period each group must turn in a hardcopy of their source code and demonstrate the completed lab using the provided test benches. Pay careful attention to the ZERO and OVERFLOW signals. An Overflow should only occur if the operation is an add, subtract or less. To receive credit each member of the group must be present for the demonstration. You are not to discuss this lab with members of other groups.

The purpose of this lab is to create and test a model of the 32-bit ALU shown in Figure 1. This ALU uses as components the one bit ALU's shown in Figure 2. Note that Ainvert, g and p have been added to the one bit ALU's. The entity alu1 models the ALU used for the low order bits and alus models the special ALU used for the sign bit.

In the provided test benchs a four-bit and two_bit version of the ALU is to be verified. For this lab, you are given on the class web page the files alu1_ans.vhd (my solution for Lab 3), alus.vhd, alu.vhd, tb_alu_V1.vhd, and tb_alu_V2.vhd. Use these files as a starting point to complete this lab. You must complete the architectures for alus and alu. The architectures for alu1 and the test benchs are complete; however, assume they are unverified and correct them if necessary. You may enhance the provided test benchs. **Do not change the entities without first obtaing approval from the instructor ot TA**. Keep all delays (including any additional logic gates that need to be added) consistent with those specified in the previous lab.

For all gates, use a delay of 1 ns. For the multiplexers and adder, use a delay of 2 ns.

Operation	op
and	00
or	01
+ (also -)	10
Result <= Less	11

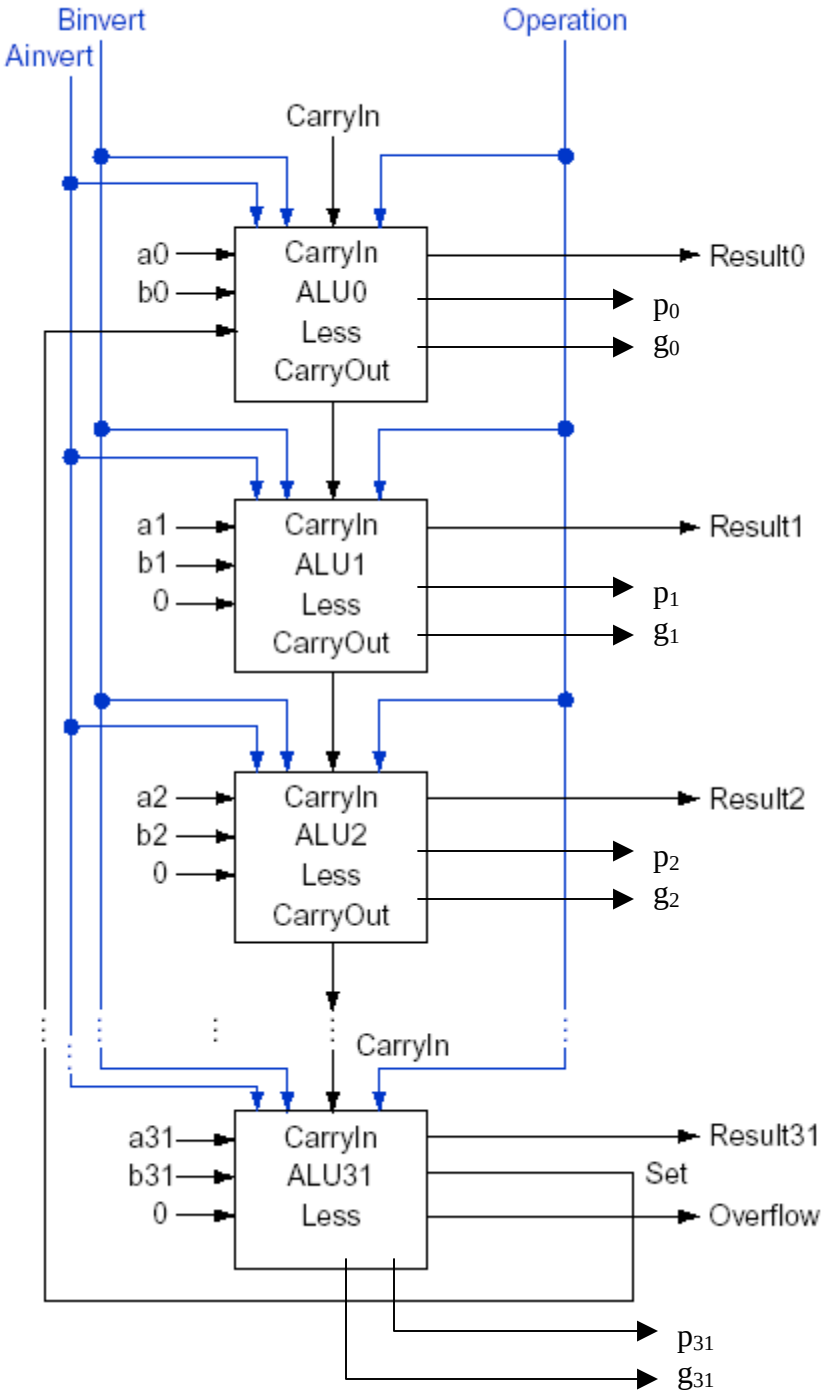

Figure 1. Structural representation of ALU.

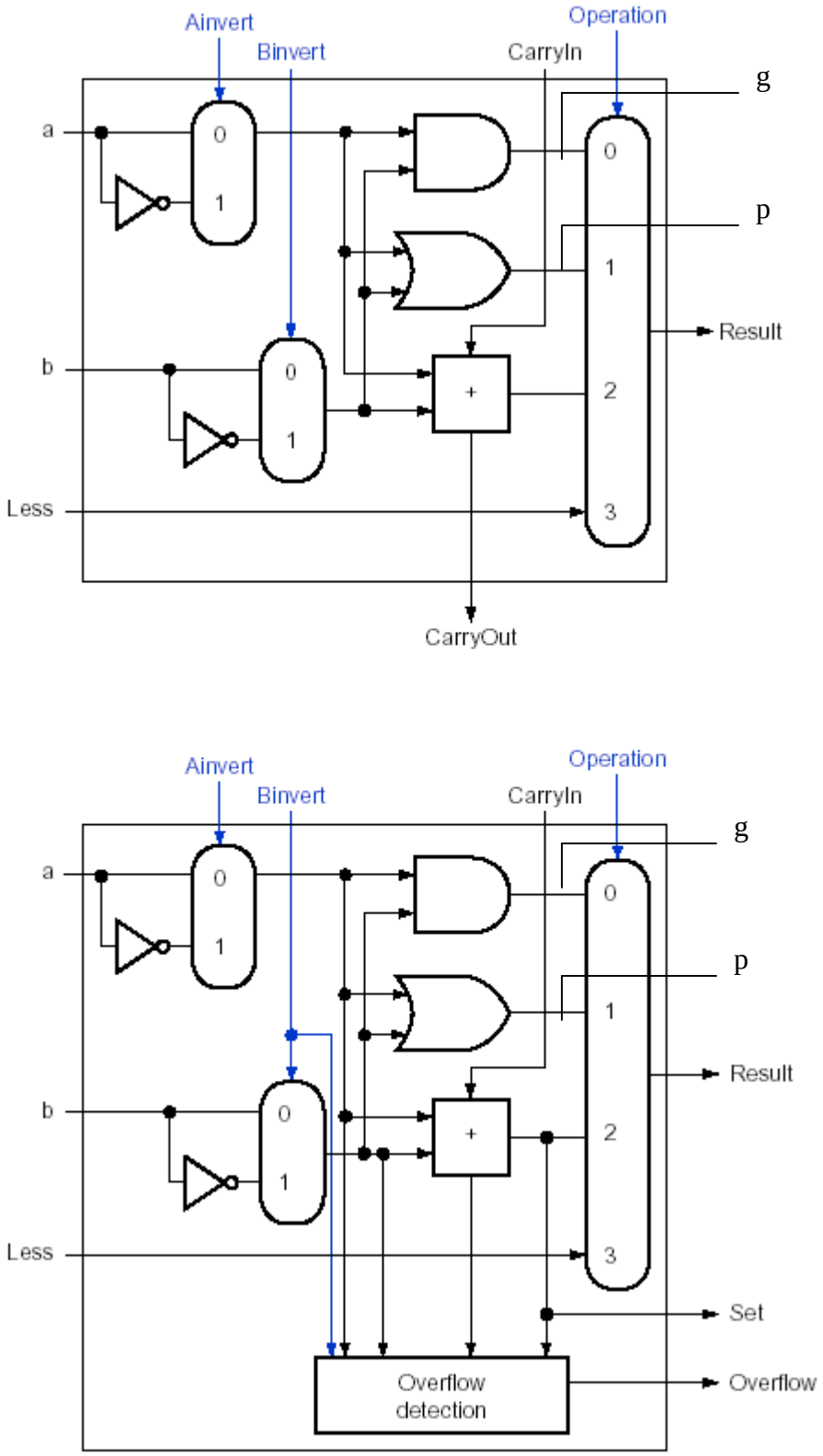

Figure 2. Alu1 in top figure and ALUs in bottom figure.