VIRGINIA COMMONWEALTH UNIVERSITY

SCHOOL OF ENGINEERING

EGRE 429 Fall 2000

VLSI Design

Credits: **4** (3 hours lecture, 2 hours laboratory)

Prerequisites: EGRE 307 Integrated Circuits and EGRE 364 Microcomputers

Instructor: Dr. Robert Klenke, Course Director
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Office Hours: W 11:00 – 12:00, TR 1:00 – 2:00

Course Web Page: http://saturn.vcu.edu/~rhklenke/egre429/index.html

Course Text: Wayne Wolf: *Modern VLSI Design – Systems on Silicon;*
Prentice Hall, 1998.

Course Description:

This is an elective course in the computer engineering sequence focusing on the design of Very Large Scale Integrated Circuits (VLSI). The primary focus is on the design techniques used for VLSI circuits, but a review of FETS and CMOS devices is included as a tool to examine tradeoffs in device parameters.

The class includes laboratory exercises, which are designed to facilitate learning the tools required to design a VLSI circuit. In order to master the material being covered during the semester, drill problems will be assigned in addition to the presented lecture material. The drill problems should be completed concurrently with the lecture material. The problems will be graded, and solutions will be made available.

Course Objectives

Upon successful completion of this course, the student will be able to:

1. Understand the function of a PMOS and NMOS field effect transistor (FET).
2. Understand the function of a CMOS inverter and the effect that variations of the device parameters have on its performance.
3. Design combinational and sequential devices using CMOS technology.
4. Integrate these types of devices into a complete VLSI system.
5. Understand the implications of advancing fabrication technology and their effect on the design of VLSI systems.
6. Design and simulate VLSI circuits using the Mentor Graphics commercial Electronic Design Automation (EDA) tools.

The course laboratory exercises involve becoming familiar with the use of Mentor Graphics commercial EDA tools in the design and analysis of VLSI devices. The cumulation of the lab exercises is a two-person project involving the design of a complete VLSI system. Completed design projects will be fabricated through MOSIS. The design projects will be documented with both a written report and an oral presentation to the class.

A course syllabus detailing the course plan, topical contents, and assignments is attached.

Laboratory Exercises

As stated above, the lab exercises are designed to help you learn the Mentor Graphics tools that are used in VLSI design. **Attendance at the laboratory periods is mandatory. Successful completion of all lab exercises is required to pass this course.**

Each lab exercise will be documented by the student with a lab write-up. The lab write-up should include the following items: 1) a brief description of lab objective and process, 2) a printout of all schematics and plots of the lab results, 3) a brief analysis of the results of the lab, 4) a description of any problems encountered, recommendations for changes, or improvements to the lab exercise. All lab exercises must be typeset and submitted in hardcopy.

Course Grading Policy

Final course grades will be determined as follows:

Quizzes (2)	15%
Homework	15%
Laboratory	10%
Class Participation	5%
Design Project	40%
Final exam	15%

There is a 10%/day “penalty” on the grade for late assignments. Class participation grade will be determined from lecture and lab attendance and the student’s participation in the in-class discussions.

Engineering Portfolios

As part of the ABET accreditation process, each student is required to maintain a portfolio of major assignments in each of their classes. For this course, the portfolio must contain, at a minimum, one of the lab write-ups and the final design project write-up.

University Policy on Cheating and Plagiarism

It is imperative that all graded assignments that you turn in during the course reflect your own understanding of the material. Copying answers from another person impedes the learning process and compromises your integrity. Students are encouraged to discuss homework problems and laboratory assignments with others, but submitted solutions must involve only an individual's effort. Any student who copies from another student's homework, quiz, exam, report, etc., or any student who knowingly allows another student to copy his or her work, or any student who submits someone else's work as his or her own, will be deemed guilty of cheating. Cheating is an extremely serious offense. Each student is expected to have read and understood the VCU Honor System Policy, as set forth in the 2000-2001 VCU Resource Guide published by the Division of Student Affairs.

For this course, the following standards for each assignment will be used:

1. Quizzes and the Final Exam will be in-class and **completely pledged** as your own work.
2. Homework must be **completely pledged** as your own work. Any assistance on the homework must be obtained from the instructor only.
3. Laboratory write-ups must be your own work and all references must be correctly cited. All schematics, layouts, and simulations must be your own work and stored in your directory. However, if you require help in using the tools, interpreting the function of the components, or debugging your design, you may obtain help from fellow students. Using or directly copying layouts obtained from the ADK library or any other source is NOT permitted.
4. The design of your portion of the final project must be ONLY the work of you and your project partner. No help from any other group or any outside source may be used without the instructor's permission.

Americans with Disabilities Act

"Section 504 of the Rehabilitation Act of 1973 and the Americans with Disabilities Act of 1990 require Virginia Commonwealth University to provide academic adjustments or accommodations for students with documented disabilities. Students seeking academic adjustments or accommodations must self-identify with the Coordinator of Services for Students with Disabilities on the appropriate campus. After meeting with the Coordinator, students are encouraged to meet with their instructors to discuss their needs, and, if applicable, any lab safety concerns related to their disabilities."

EGRE 429 **Fall 2000**

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Course Syllabus – **subject to change if necessary**.
Note that the withdrawal date is **October 20th** according to the Academic Calendar published in the 2000-2001 VCU Bulletin.

Day	Topic	Reading Assignment	Notes
Tuesday, Aug. 29th	Class overview and Introduction	Chapter 1	Problem 1.3 – except assume 20 million transistors, 1/3 in cache, and 64 bit processor width
Thursday, Aug. 31st	Transistors and Layout	Chapter 2	Problems 2.2, 2.3, 2.7, 2.8, 2.11
Lab 1	Lab 1 - Functional Simulation with Accusim	Lab Handout	
Tuesday, Sept. 5th	Transistors and Layout	Chapter 2	
Thursday, Sept. 7th	Logic Gates	Chapter 3	Problems 3.1, 3.2, 3.12
Lab 2	Lab 2 – Full Custom Design of a CMOS Inverter	Lab Handout	Group and Project Selection due *Wednesday, Sept. 6th*
Tuesday, Sept. 12th	Logic Gates	Chapter 3	
Thursday, Sept. 14th	Logic Gates	Chapter 3	
Lab 3	Full Custom Design of a CMOS Inverter (cont.)	Lab Handout	
Tuesday, Sept. 19th	Combinational Logic Networks	Chapter 4	Problems 4.2, 4.3, 4.4, and size transistors in 3.2 solution for equal rise & fall times
Thursday, Sept. 21st	Combinational Logic Networks	Chapter 4	
Lab 4	Lab 4 – Schematic Driven Layout	Lab Handout	Initial Area and Shape Estimate due *Monday, September 18th*

Tuesday, Sept. 26th	Combinational Logic Networks	Chapter 4	
Thursday, Sept. 28th	Combinational Logic Networks	Chapter 4	
Lab 5	Lab 5 – Hierarchical Design	Lab Handout	
Tuesday, Oct. 3rd	No class		
Thursday, Oct. 5th	Quiz #1		
Lab 6			
Tuesday, Oct. 10th	Sequential Machines	Chapter 5	Problems 5.2, 5.4 (use SR FF as basis, layout with ICStation & simulate w/ MachTA)
Thursday, Oct. 12th	Sequential Machines	Chapter 5	
Lab 7	Design Project		
Tuesday, Oct. 17th	Sequential Machines	Chapter 5	
Thursday, Oct. 19th	Sequential Machines	Chapter 5	
Lab 8	Design Project		Preliminary Design Report due *Monday, October 16th*
Tuesday, Oct. 24th	Subsystem Design	Chapter 6	In-class project reports
Thursday, Oct. 26th	Subsystem Design	Chapter 6	Problem 6.7, 6.13
Lab 9	Design Project		
Tuesday, Oct. 31st	Subsystem Design	Chapter 6	In-class project reports
Thursday, Nov. 2nd	Subsystem Design	Chapter 6	
Lab 10	Design Project		
Tuesday, Nov. 7th	Subsystem Design	Chapter 6	In-class project reports
Thursday, Nov. 9th	Quiz #2		
Lab 11	Design Project		

Tuesday, Nov. 14th	Floorplanning	Chapter 7	In-class project reports
Thursday, Nov. 16th	Floorplanning	Chapter 7	
Lab 12	Design Project		Initial Layout and Testing Complete *Monday, November 13th*
Tuesday, Nov. 21st	Floorplanning	Chapter 7	In-class project reports
Thursday, Nov. 23rd	Holiday (no class)		
Lab 13	Design Project		
Tuesday, Nov. 28th	Architecture Design	Chapter 8	
Thursday, Nov. 30th	Architecture Design	Chapter 8	
Lab 14	Design Project		Super-block Layout and Testing Complete *Monday November 27th*
Tuesday, Dec. 5th	CAD Systems and Algorithms	Chapter 10	
Thursday, Dec. 7th	CAD Systems and Algorithms	Chapter 10	
Lab 15	Design Project		Final Chip Layout and Testing Complete – final reports due *Thursday, December 7th*