MicroBlaze Tutorial #1

For this first tutorial we will set up a simple example using the Digilab DE2 board with the DIO1 board connected to the A and B connectors. This setup is shown below:

The switches on the DIO1 board are read and output to the LED's.



Select File \rightarrow New Project \rightarrow Platform Studio.

Create New Proje	ect		
New Project The project file will	be created in the curr	ent directory if a p	ath is not specified.
Project File	C:\MB_Tutorials\T1	\system.xmp	Browse
Existing MHS to Import (Optional)			Browse
Target Device	Device Size	Package	Speed Grade
spartan2e 💌	хс2ѕ200€ ▼	pq208 💌	-6 💌
Peripheral Reposito	ory Directory I Repository search pa colon separated list of	ath for IP, driver ar directories.	nd library files.
			Browse
		OK	Cancel

Specify project file location, spartan2e, xcs2s200e, pg208, speed –6. Click on OK.



Click on Yes. Then on OK.

S Xilinx XPS - C:\MB_Tutorials\T1\						
File Edit View Project Tools Options Window Help						
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System Options Symbols						
Right Click for Options						
Bystem BSP □ B Project Files ■ MHS File: system.mhs ■ MSS File: system.mss						



Add the following components:

- 1. microblaze
- 2. bram_block
- 3. opb_gpio
- 4. opb_gpio
- 5. lmb_bram_if_cntlr
- 6. lmb_bram_if_cntlr
- 7. opb_jtag_uart

Rename the peripherals Instance name and change the addresses as shown below.

Peripheral	HW Ver	Instance	Base Address	High Address
microblaze	2.00.a	mblaze		
bram_block	1.00.a	bram1		
opb_gpio	2.00.a	gpio_swts	0xfffe0400	0xfffe05ff
opb_gpio	2.00.a	gpio_leds	0xfffe0600	0xfffe07ff
lmb_bram_if_cntlr	1.00.b	lmb_d_cntrl	0x0000000	0x00000fff
lmb_bram_if_cntlr	1.00.b	lmb_i_cntrl	0x0000000	0x00000fff
opb_jtag_uart	1.00.b	jtag_uart	0xffff8000	0xffff80ff

eripherals Bus	Connection	s Ports Para	enters edited.	ick Delete	
Peripheral	HW Ver	Instance	Base Address	High Address	Min
microblaze	2.00.a 🔹	mblaze			
bram_block	1.00.a	bram1			
opb_gpio	3.00.a 💌	gpio_swts	0xfffe0400	0xfffe05ff	0x2
opb_gpio	3.00.a 💌	gpio_leds	0xfffe0600	0xfffe07ff	0x2
lmb_bram_i	1.00.b	Imb_d_cntrl	0x00000000	0x00000fff	0x8
lmb_bram_i	1.00.b	Imb_i_cntrl	0x00000000	0x00000fff	0x8
oph itag u	1.00 h	itag uart	0xEEEE8000	0xEEEE80EE	1

Select the Bus Connections tab, and add one instance of opb_v20_v10_a and two instances of lmb_v10_v1_00_a. By right clicking rename these to opb, d_lmb, and I_lmb. Changes the connectors to PORTA and PORTB, and set up the master slave connections as shown below.

Add/Edit Hardwa	re F	lati	forn	n Spe	cifications					×
Peripherals Bus Co	onne	ction	s F	orts	Parameters					,
Click on squares to Right click on any	o mał bus i	ce mi nstar	aster nce (; slave (colum	e or master-slave (M, S, MS) co n header) for a context menu.	nnections.		Choose one or more buses and click Add	(using shiftand Ctrl) a	_
mblaze dlmb		м						isocm v10 v1 00	b	
mblaze ilmb			м			<< Add		opb_v20_v1_10_a		
mblaze dopb	м					2		plb_v34_v1_01_a		~
mblaze iopb	М					Choose the BRAM p	ort to	connect to the contro	oller port.	
gpio_swts sopb	8					Give a name to the o	conne	ection.		
gpio_leds sopb	0					Cntlr Port	BRA	M Port	Connector	-
Imb_d_ontri simb	65 - 67	s				lmb_d_cntrl bra	bran	11 PORTA	PORTA	
Imb_i_cntrl sImb	26 - 39 38 - 38		s			Imb_i_cntrl bra	bran	1 PORTB	PORTB	
jtag_uart sopb	s									

Select the Ports tab and enter the values as shown below. Be sure to set the range as [0:7] for the GPIO_IO ports.



The final configuration should is shown below. Click Apply when done.

Instance	Port Name	Net Name	Pol	Scope	Ra	Class	Sensit
mblaze	CLK	sys_clk	I	Ext 💌		CLK	
mblaze	INTERRUPT	net_gnd	I	Inte 💌		INTER	LEVEL
gpio_swts	GPIO_IO	swts	IO	Ext 💌	[0:7]		
gpio_leds	GPIO_IO	leds	IO	Ext 💌	[0:7]		
opb	OPB_Clk	sys_clk	I	Ext 💌		CLK	
opb	SYS_Rst	sys_reset	I	Ext 💌	1		
d_lmb	LMB_Clk	sys_clk	I	Ext 💌	1	CLK	
d_lmb	SYS_Rst	sys_reset	I	Ext 💌			
i_lmb	LMB_Clk	sys_clk	I	Ext 💌		CLK	
i_lmb	SYS_Rst	sys_reset	I	Ext 💌			

Select Parameters tab. Select gpio_swts and add C_GPIO_WIDTH and change the value to 8. Repeat the same process with gpio_leds.

.dd/Edit Hardware Pla	atform Sp	ecifications			
Peripherals Bus Connecti	ions Ports	Parameters			
Edit Parameters assigned	to IP Instan	ce in MHS		Choose IP Instance for a	list of para
These parameter values v	will override o	default MPD values.		gpio_leds	
Parameter	Valu	Je	_	Parameters with default v Choose one or more (usin	alues from ig shift and
C_GPIO_WIDTH	8			Parameter	Value
			C	C_USER_ID_CODE	3
			- N.	C_DW	32
				C_AW	32
				C CRIO WIDTH	22

Click on Apply and OK.

By selecting Project \rightarrow View Schematic you can be a schematic representation of the architecture.



Create a directory "code" in the project directory and save the program below as system.c in the code directory.

Select the System tab then highlight mblaze.



Select system.c in the code directory.

Add Source	and Header Files to the current	proce	ssor	? 🗙
Look in:	code 💌	-	D 💣	 ▼
C system.c				
-				
File <u>n</u> ame:	system.c			<u>O</u> pen
Files of type:	Program Files (*.c,*.s,*.cc,*.cpp,*.cxx,*.c	***,* 💌		Cancel

You may edit the program within the XPS by selecting system.c under Sources as shown.

Xilinx XPS - C:\MB_Tutorials\T1\ - [system.c]
😽 File Edit View Project Tools Options Window I	Help
」D 📽 🖬 🖉 🚭 🗍 % 🖻 🛍 ∾ ∾ 🕅] &
<u> </u>	00 /***********************************
System Options Components	01 * Microblaze demostration using the Dig
	02 * Outputs switches to Led's.
Right Click for Options	04 * Date: 12/21/03
🖃 🏥 System BSP 🛛 🔼	05 * Project: MB_PIO connects switches to
🛱 🖓 mblaze	07 ************************************
Debug Peripheral:	08 #include "xparameters.h"
Mode:	10 woid main(int argc_char *argv[])
	11 {
Inter Script:	12 13 VCpic mSetDataDirection/VDAD CDIO (
Generated Header: mblaze/include	14 XGpio_mSetDataDirection(XFAR_GFIO_
⊡-@ Sources	15 while (1)
C:\MB_Tutorials\T1\code\system.c	17 1/* tie switches to the leds */
Headers	18 XGpio_mSetDataReg(XPAR_GPIO_LE)
trami	19 XGpio_mGetDatal
the second secon	21
The second secon	22 }
I Inb i cntrl	

The .ucf file is used to map the signal to the appropriate pins of the FPGA.

If necessary create a data directory and add a system.ucf containing the information shown below.

NET "sys_clk" LOC = "P80";	# 50 MHz
NET "sys_reset" LOC = "P40";	#BTN1 on DIO board
NET "leds<0>" LOC = "P44";	#LED0
NET "leds<1>" LOC = "P46";	#LED1
NET "leds<2>" LOC = "P48";	#LED2
NET "leds<3>" LOC = "P55";	#LED3
NET "leds<4>" LOC = "P57";	#LED4
NET "leds<5>" LOC = "P59";	# LED5
NET "leds<6>" LOC = "P61";	#LED6
NET "leds<7>" LOC = "P63";	# LED7
NET "swts<0>" LOC = "P16";	# SWT0
NET "swts<1>" LOC = "P18";	# SWT1
NET "swts<2>" LOC = "P21";	# SWT2
NET "swts<3>" LOC = "P23";	# SWT3
NET "swts<4>" LOC = "P27";	# SWT4
NET "swts<5>" LOC = "P30";	# SWT5
NET "swts<6>" LOC = "P33";	# SWT6
NET "swts<7>" LOC = "P35";	# SWT7

Select Tools \rightarrow Clean \rightarrow All to delete unneeded files. This step is not necessary the first time, but may be required if changes are made.

B_Tu	torials\T1\ - [system.c]			
oject	Tools Options Window Help	24		
∦ ∦	Generate <u>L</u> ibraries <u>C</u> ompile Program Sources Get <u>P</u> rogram Size Generate BSP for <u>V</u> xWorks	Q X X Q ⊈ ℃ ‰ 秒 %		
ompon Jlick fc	Generate <u>N</u> etlist Generate <u>B</u> itstream Generate SystemACE File Import Peripheral Wizard	<pre>/********* * Microbla * Outputs * Author: * Date: * Project: *</pre>		
Peripl	<u>U</u> pdate Bitstream <u>D</u> ownload	tinclude "s		
TO See C	Clean 🕨	Libraries "x		
: JT: Script:	Sim <u>M</u> odel Generation <u>H</u> ardware Simulation	Program n.(Netlist Bits n		
sted H >s vMB_T rs —	XMD	Simulation		
	<u>S</u> oftware Debugger X <u>y</u> gwin shell	Software Hardware		
43 4	Terminate Process	All		
	20 C			

Using the Tools menu successively select the following: Generate Libraries, Compile Program Source, Generate Netlist, Generate Bitstream, Update Bitstream. Alternatively you may successively select the icons shown below.

B_Tu	torials\T1\ - [system.c]		1000			1.5
oject	Tools Options Window He	lp	1		1	P
ال [[] الله ال	Generate Libraries Compile Program Sources Get Program Size Generate BSP for VxWorks	Q 21	- Hibe	٢		BRAF
ompon Xlick fc	Generate <u>N</u> etlist Generate <u>B</u> itstream Generate SystemACE File Import Peripheral Wizard					
Peripl	Update Bitstream Download Clean					
: JT: Script:	Sim <u>M</u> odel Generation <u>H</u> ardware Simulation					
ated H >s \MB_T rs	<u>X</u> MD <u>S</u> oftware Debugger X <u>y</u> gwin shell					

At this point the download.bit file has been crated in the implementation directory of the project.



With the parallel cable connected between the PC and the DE2 board, start the impact program. Note: Impact.exe is located in the directory where the ISE was installed, usually at "c:\Xilinx\bin\nt\impact.exe".

Operation Mode Selection	×
What do you want to do first?	
Configure Devices	
C Prepare Configuration Files	
C Load Configuration File (.cdf, .pdr)	
< <u>B</u> ack <u>N</u> ext > Cancel Help	

Click on Cancel

With Boundary-Scan selected, right click to bring up menu and select Add Xilinx Device. In the project's implementation directory, select download.bit.



Place cursor over Xilinx chip and right click to select program to download the download.bit file.

