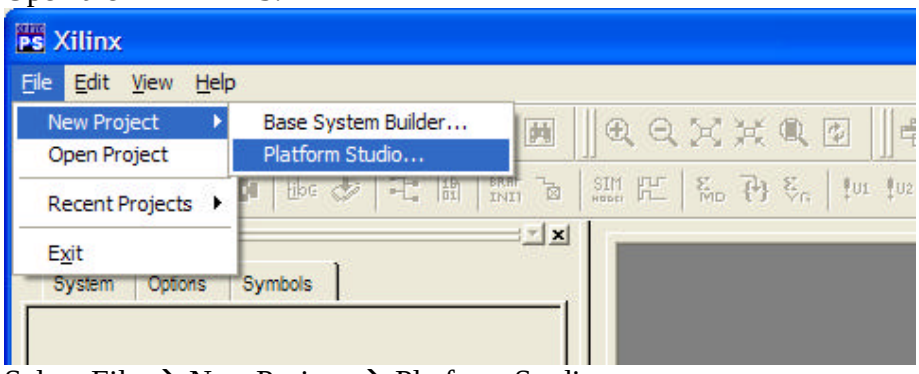
MicroBlaze Tutorial # 1

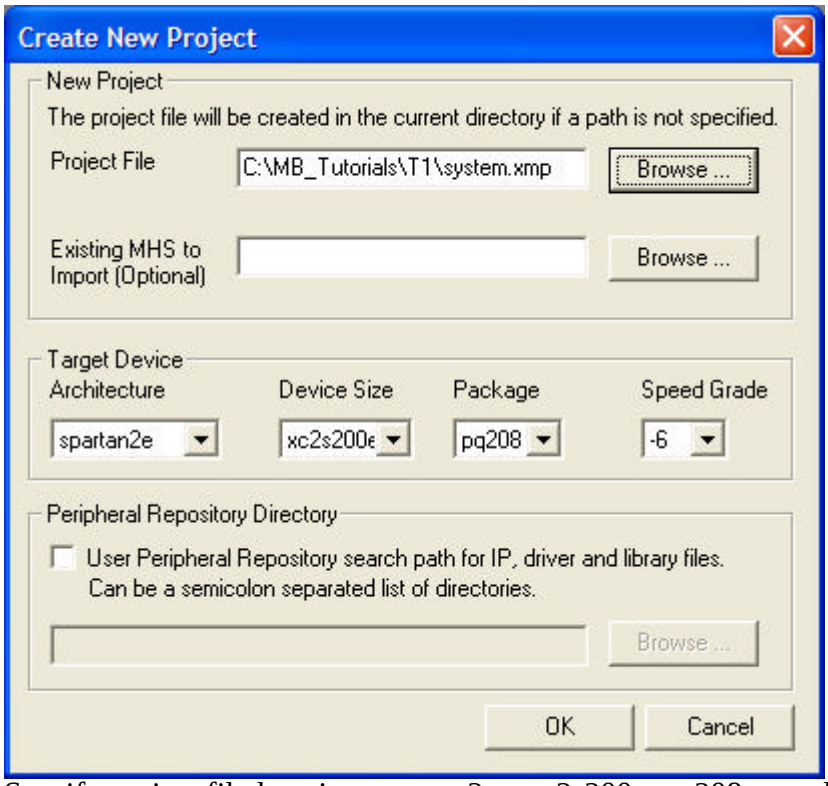
For this first tutorial we will set up a simple example using the Digilab DE2 board with the DIO1 board connected to the A and B connectors. This setup is shown below:

The switches on the DIO1 board are read and output to the LED's.

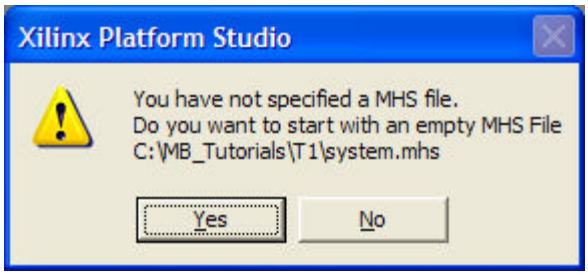

Open the Xilinx XPS.



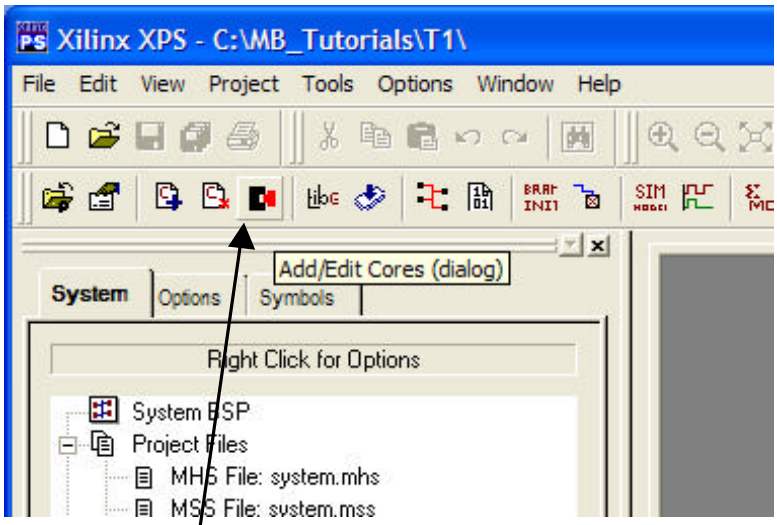

Select File → New Project → Platform Studio.




Specify project file location, spartan2e, xcs2s200e, pg208, speed –6. Click on OK.



Click on Yes. Then on OK.



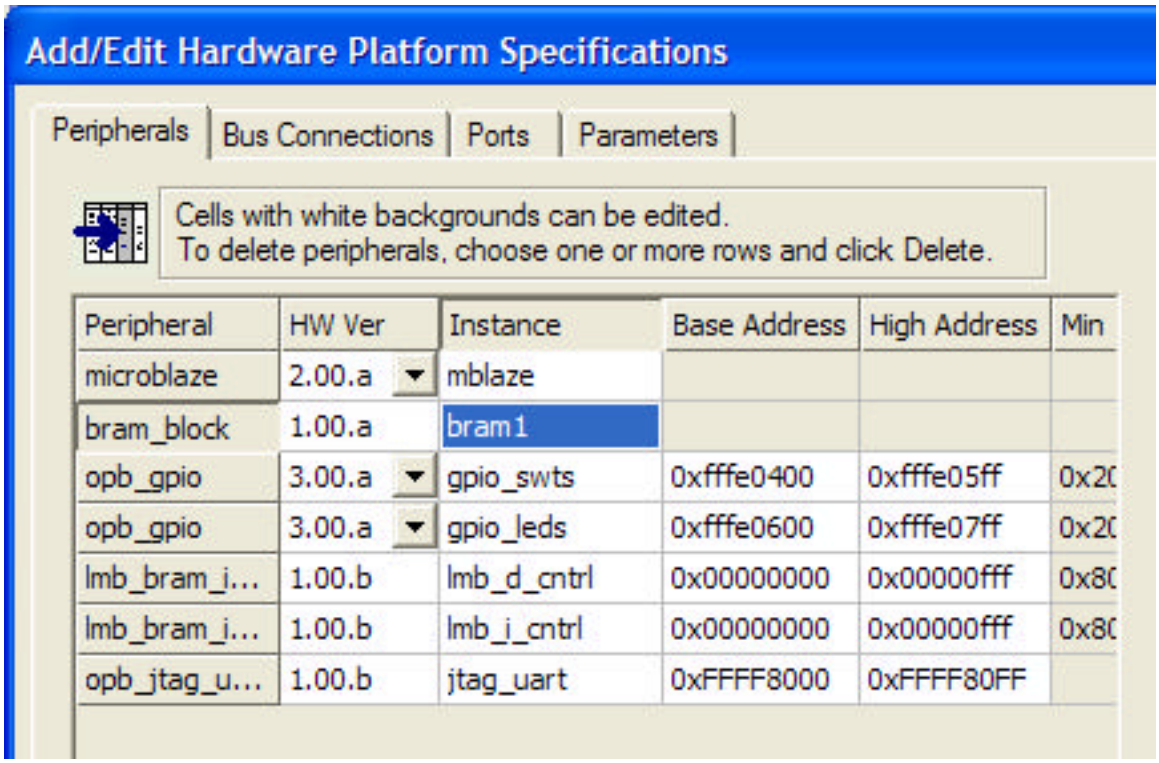

Click on "Add/Edit Cores" icon or select Project → Add/Edit Cores.

Add the following components:

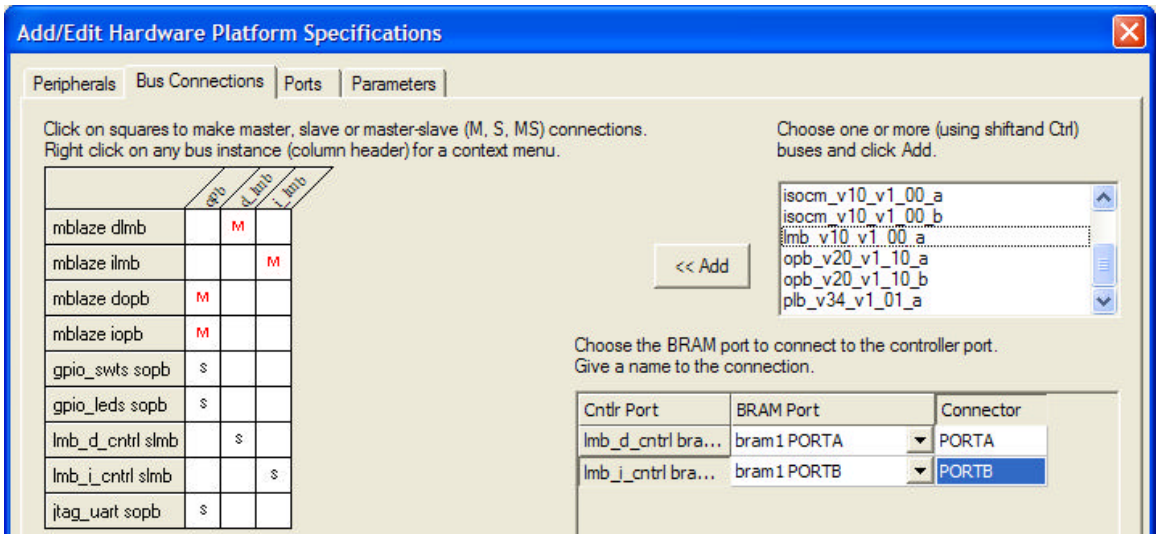
1. microblaze
2. bram_block
3. opb_gpio
4. opb_gpio
5. lmb_bram_if_cntlr
6. lmb_bram_if_cntlr
7. opb_jtag_uart

Rename the peripherals Instance name and change the addresses as shown below.

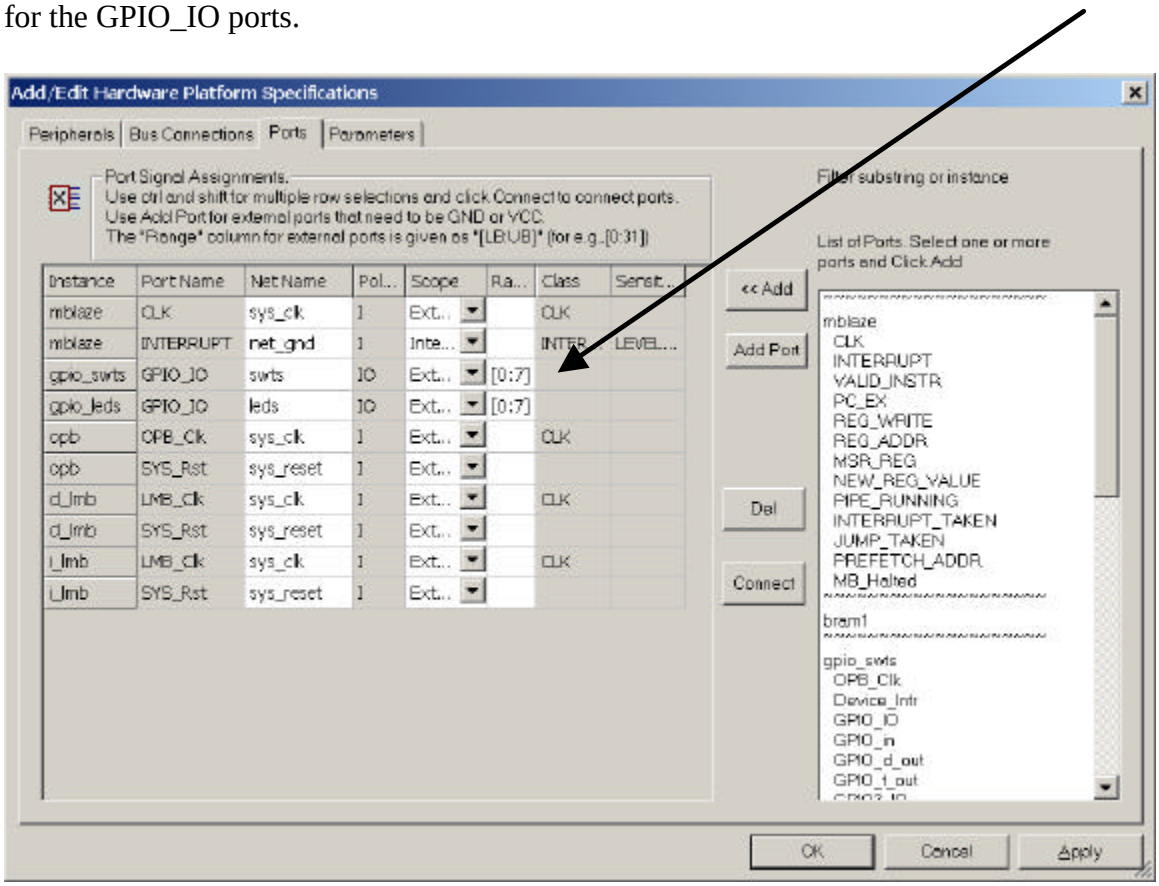
| Peripheral | HW Ver | Instance | Base Address | High Address |
|---|---|---|---|---|
| microblaze | 2.00.a | mblaze | | |
| bram_block | 1.00.a | bram1 | | |
| opb_gpio | 2.00.a | gpio_swts | 0xfffe0400 | 0xfffe05ff |
| opb_gpio | 2.00.a | gpio_leds | 0xfffe0600 | 0xfffe07ff |
| lmb_bram_if_cntlr | 1.00.b | lmb_d_cntrl | 0x00000000 | 0x00000fff |
| lmb_bram_if_cntlr | 1.00.b | lmb_i_cntrl | 0x00000000 | 0x00000fff |
| opb_jtag_uart | 1.00.b | jtag_uart | 0xffff8000 | 0xffff80ff |




Select the Bus Connections tab, and add one instance of opb_v20_v10_a and two instances of lmb_v10_v1_00_a. By right clicking rename these to opb, d_lmb, and I_lmb. Changes the connectors to PORTA and PORTB, and set up the master slave connections as shown below.



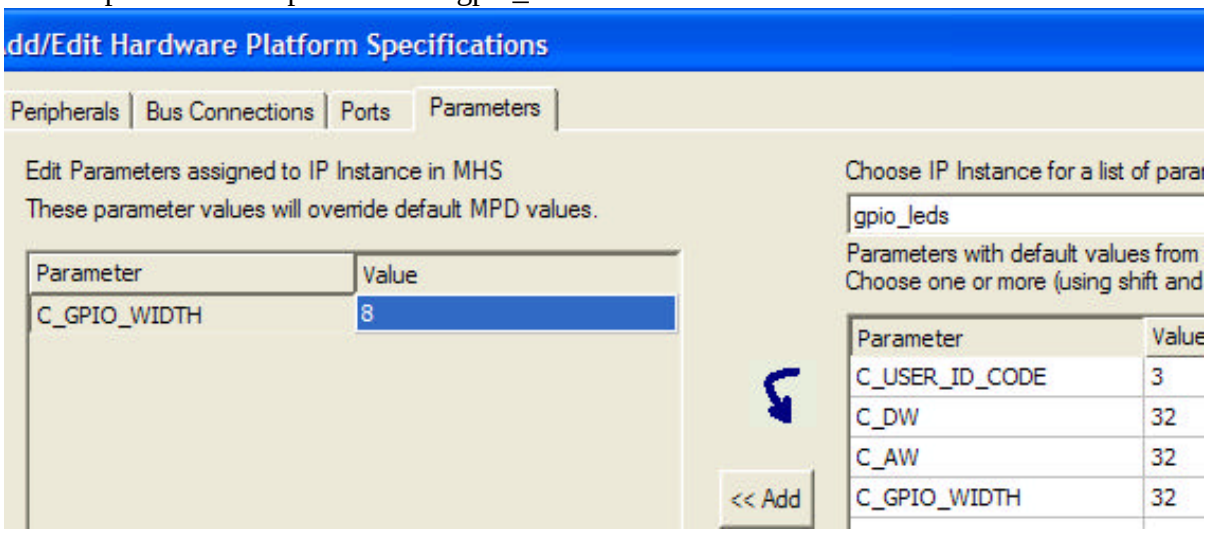
Select the Ports tab and enter the values as shown below. Be sure to set the range as [0:7] for the GPIO_IO ports.




The final configuration should is shown below. Click Apply when done.

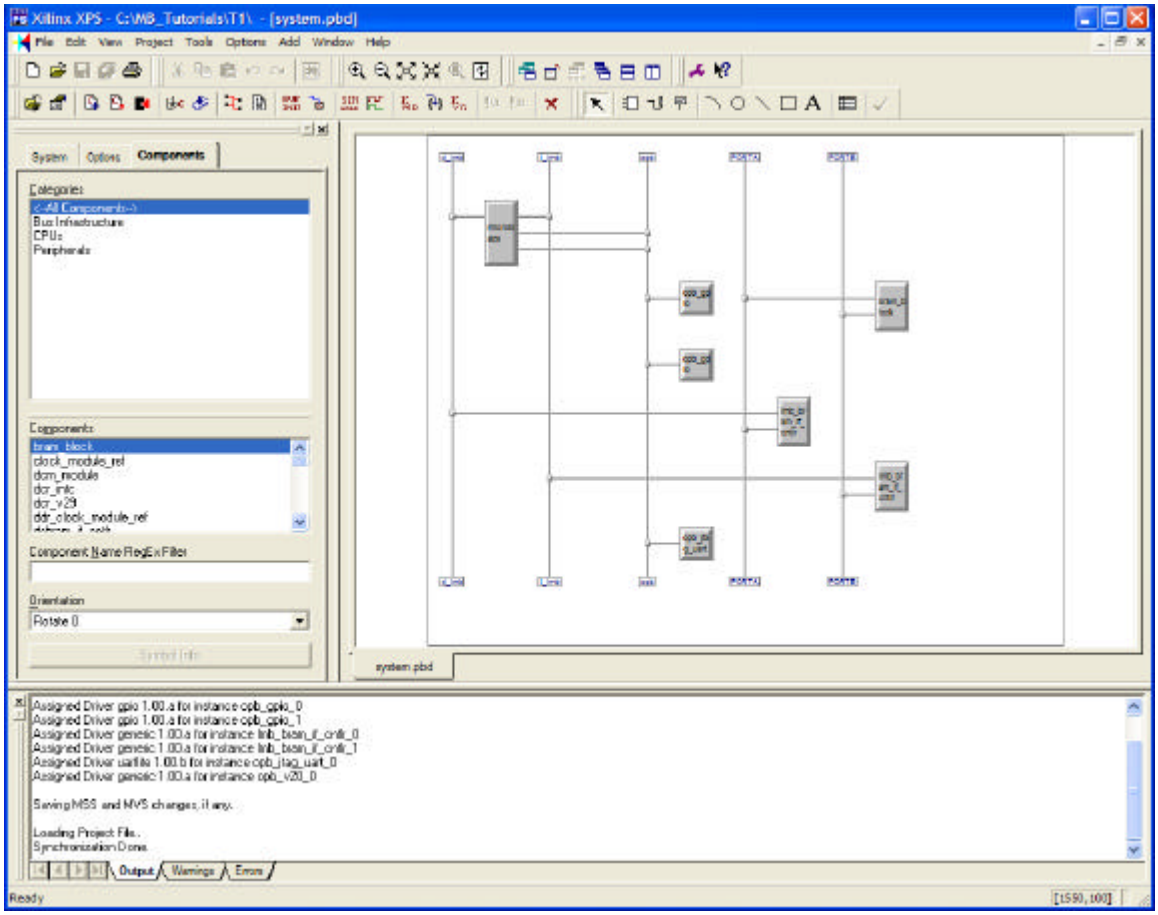
| Instance | Port Name | Net Name | Pol... | Scope | Ra... | Class | Sensit... |
|---|---|---|---|---|---|---|---|
| mblaze | CLK | sys_clk | I | Ext... | | CLK | |
| mblaze | INTERRUPT | net_gnd | I | Inte... | | INTER... | LEVEL... |
| gpio_swts | GPIO_IO | swts | IO | Ext... | [0:7] | | |
| gpio_leds | GPIO_IO | leds | IO | Ext... | [0:7] | | |
| opb | OPB_Clk | sys_clk | I | Ext... | | CLK | |
| opb | SYS_Rst | sys_reset | I | Ext... | | | |
| d_lmb | LMB_Clk | sys_clk | I | Ext... | | CLK | |
| d_lmb | SYS_Rst | sys_reset | I | Ext... | | | |
| i_lmb | LMB_Clk | sys_clk | I | Ext... | | CLK | |
| i_lmb | SYS_Rst | sys_reset | I | Ext... | | | |

Select Parameters tab. Select gpio_swts and add C_GPIO_WIDTH and change the value to 8. Repeat the same process with gpio_leds.




Click on Apply and OK.

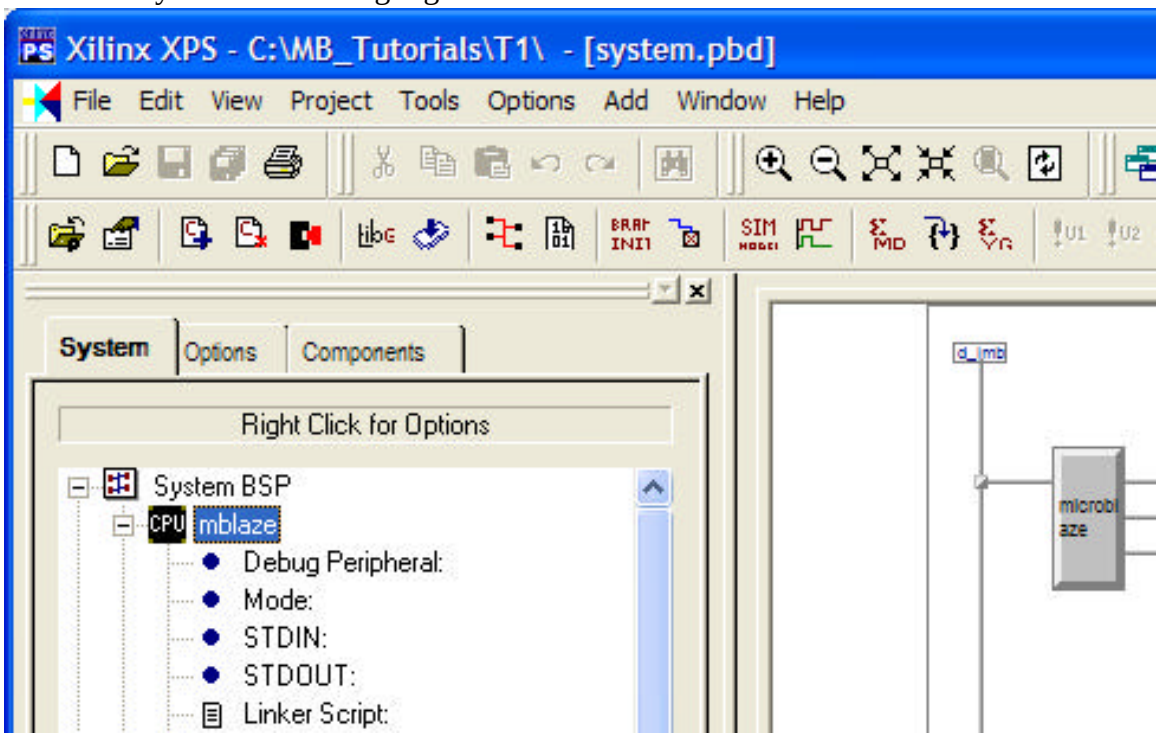
By selecting Project → View Schematic you can be a schematic representation of the architecture.



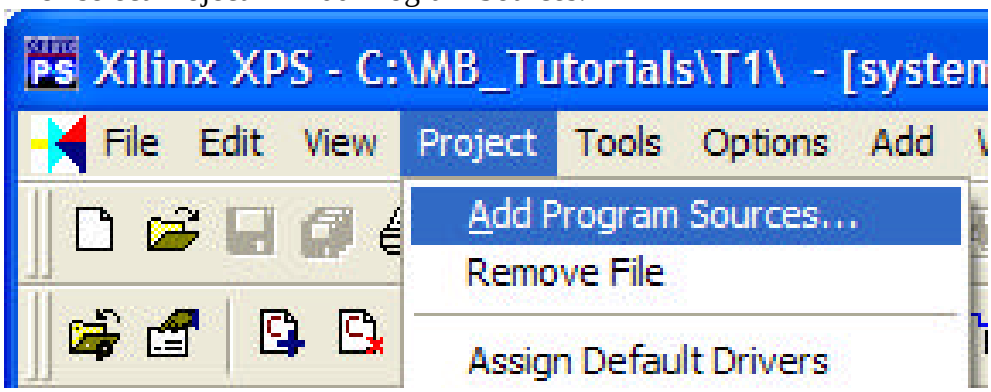
Create a directory “code” in the project directory and save the program below as system.c in the code directory.

```
#include "xparameters.h"
#include "xgpio_l.h"
void main(int argc, char *argv[])
{           XGpio_mSetDataDirection(XPAR_GPIO_SWTS_BASEADDR, 0xFF);
            XGpio_mSetDataDirection(XPAR_GPIO_LEDS_BASEADDR, 0x00);
   while (1)
   {
       XGpio_mSetDataReg(XPAR_GPIO_LEDS_BASEADDR,
                   XGpio_mGetDataReg(XPAR_GPIO_SWTS_BASEADDR));
   }
}
```

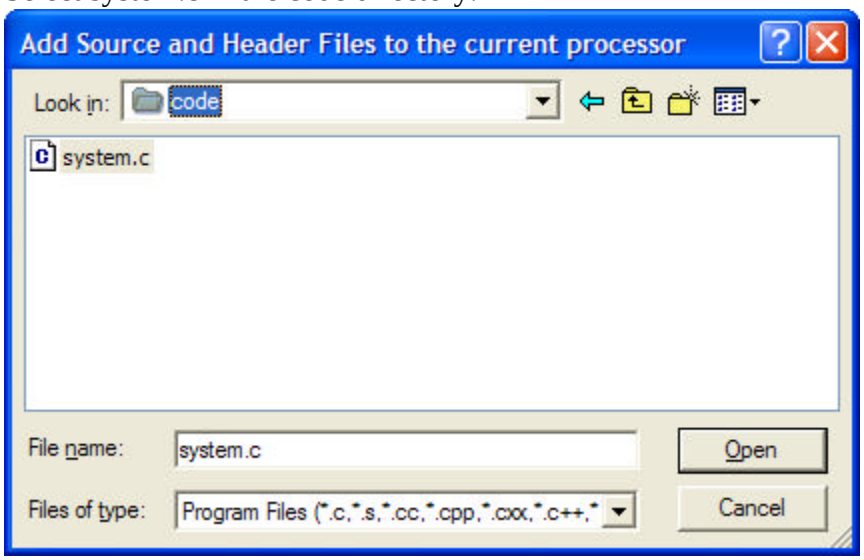
Select the System tab then highlight mblaze.



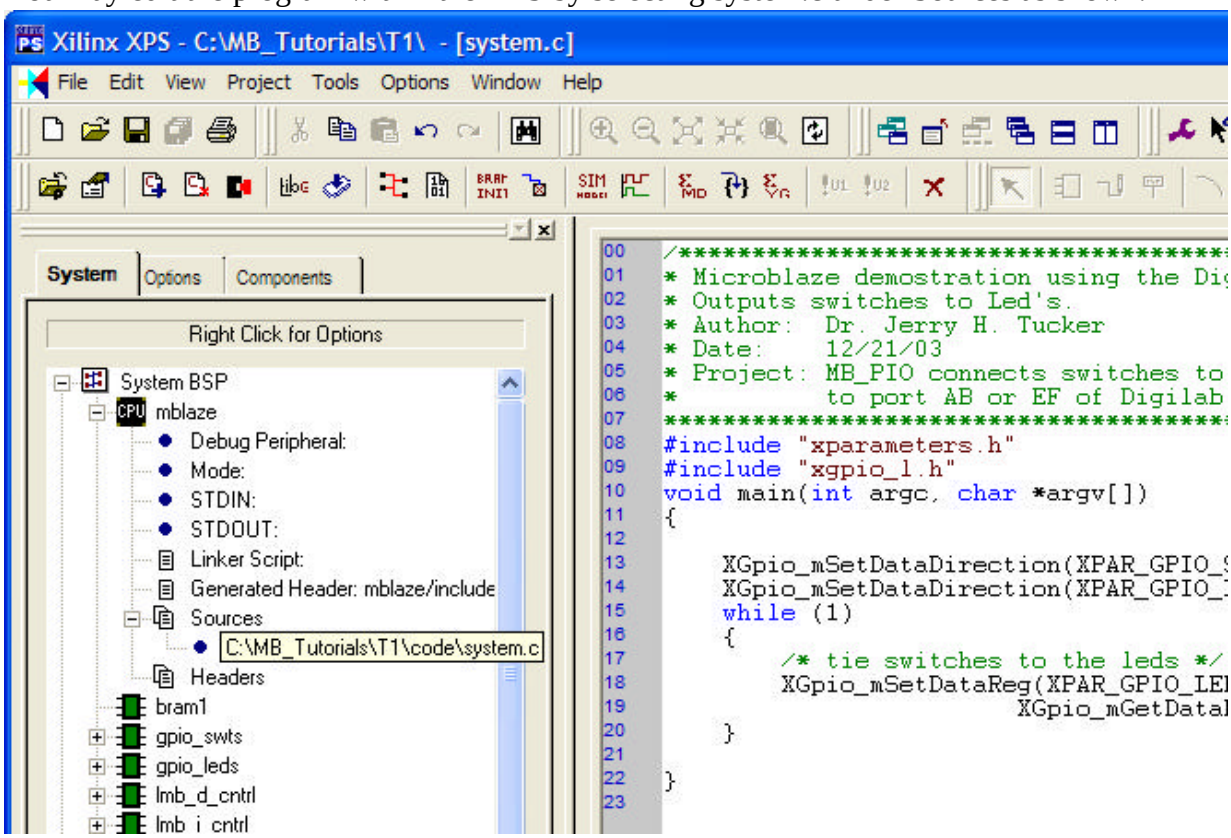

Then select Project → Add Program Sources.



Select system.c in the code directory.



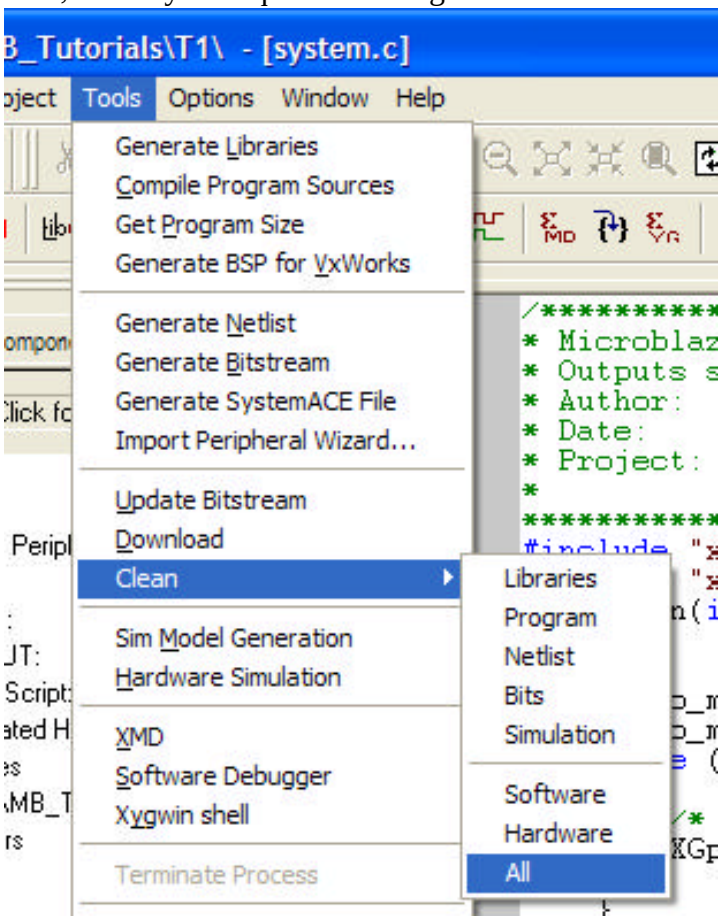

You may edit the program within the XPS by selecting system.c under Sources as shown.



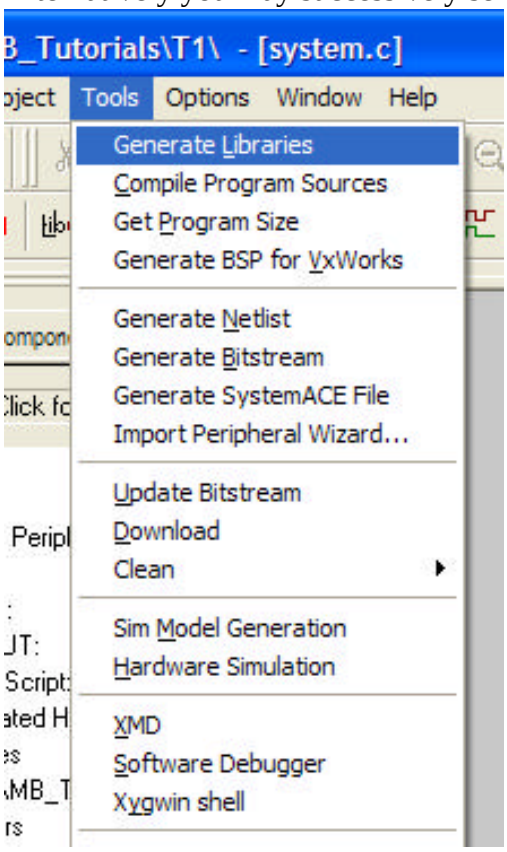
The .ucf file is used to map the signal to the appropriate pins of the FPGA.
If necessary create a data directory and add a system.ucf containing the information shown below.

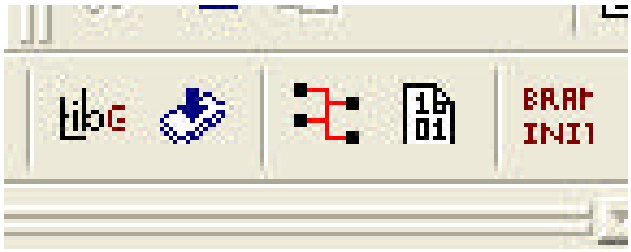
```
NET "sys_clk"  LOC = "P80";      # 50 MHz
NET "sys_reset" LOC = "P40";     # BTN1 on DIO board
NET "leds<0>" LOC = "P44";       # LED0
NET "leds<1>" LOC = "P46";       # LED1
NET "leds<2>" LOC = "P48";       # LED2
NET "leds<3>" LOC = "P55";       # LED3
NET "leds<4>" LOC = "P57";       # LED4
NET "leds<5>" LOC = "P59";       # LED5
NET "leds<6>" LOC = "P61";       # LED6
NET "leds<7>" LOC = "P63";       # LED7
NET "swts<0>" LOC = "P16";       # SWT0
NET "swts<1>" LOC = "P18";       # SWT1
NET "swts<2>" LOC = "P21";       # SWT2
NET "swts<3>" LOC = "P23";       # SWT3
NET "swts<4>" LOC = "P27";       # SWT4
NET "swts<5>" LOC = "P30";       # SWT5
NET "swts<6>" LOC = "P33";       # SWT6
NET "swts<7>" LOC = "P35";       # SWT7
```

Select Tools → Clean → All to delete unneeded files. This step is not necessary the first time, but may be required if changes are made.



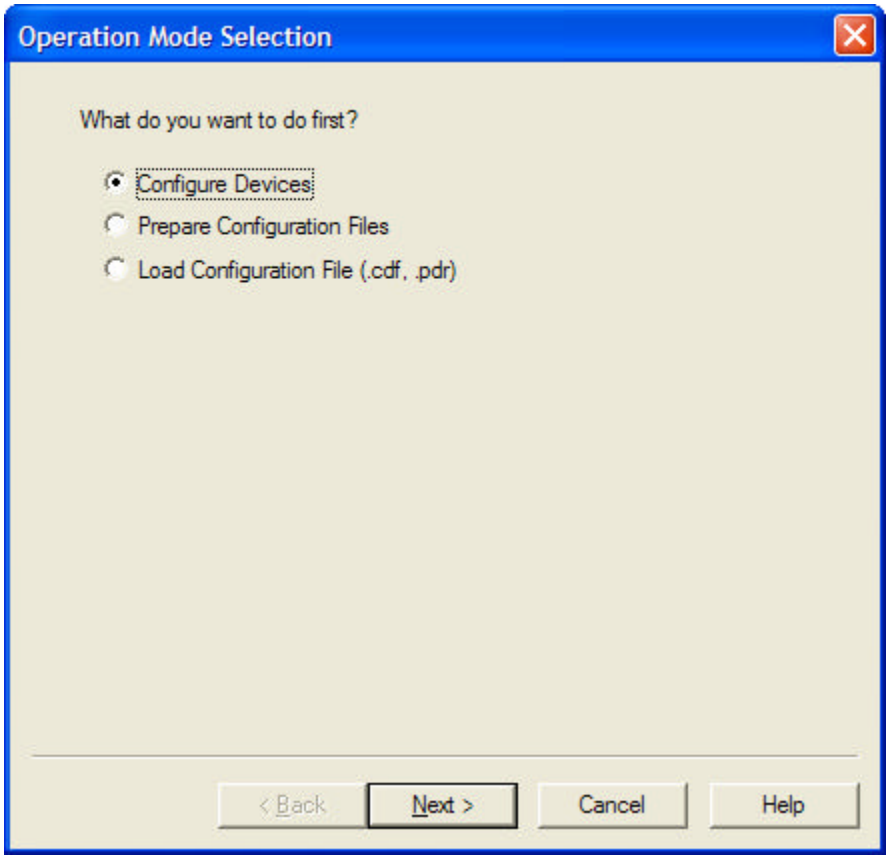
Using the Tools menu successively select the following: Generate Libraries, Compile Program Source, Generate Netlist, Generate Bitstream, Update Bitstream. Alternatively you may successively select the icons shown below.



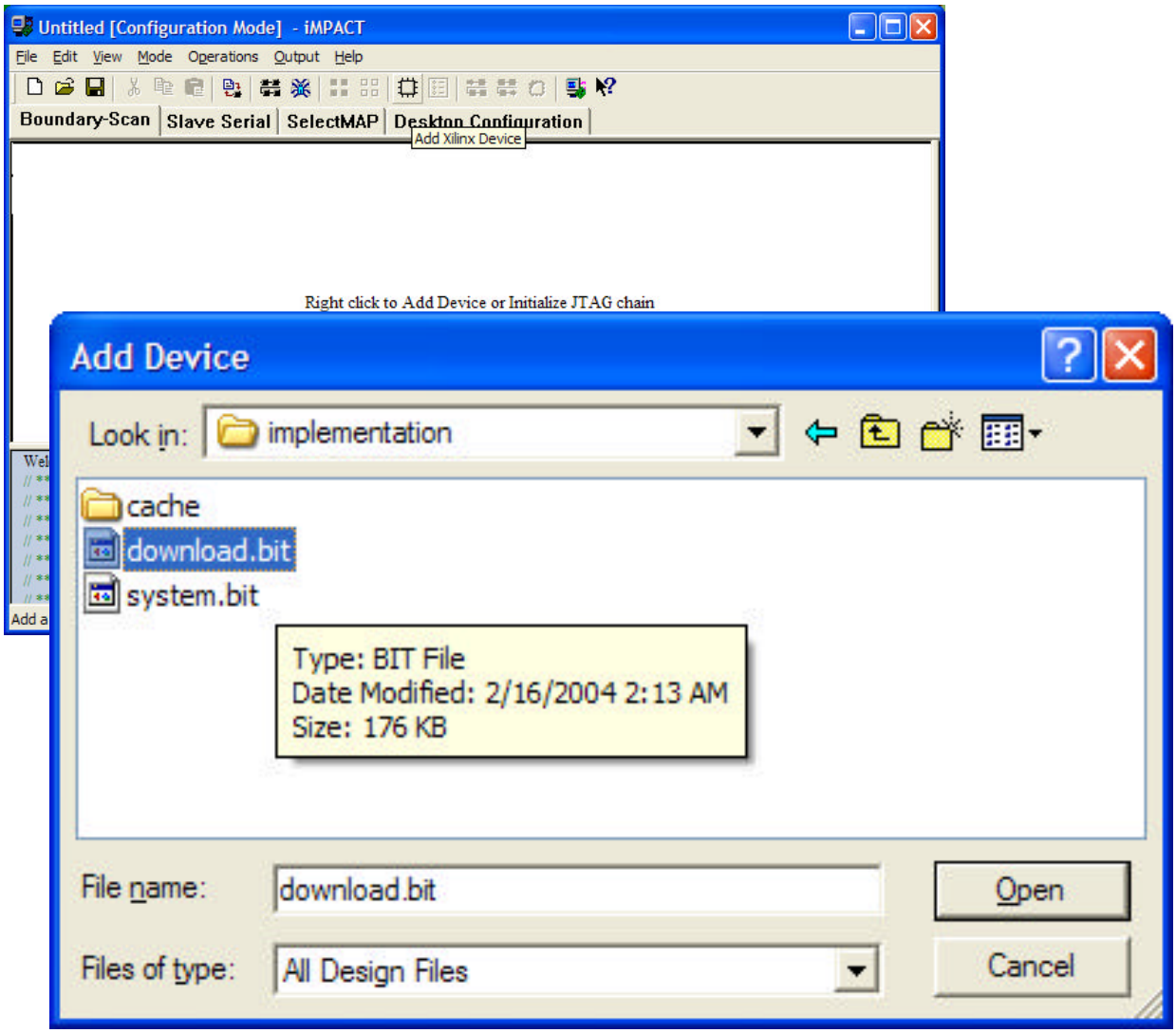
At this point the download.bit file has been crated in the implementation directory of the project.


With the parallel cable connected between the PC and the DE2 board, start the impact program. Note: Impact.exe is located in the directory where the ISE was installed, usually at "c:\Xilinx\bin\nt\impact.exe".




Click on Cancel

With Boundary-Scan selected, right click to bring up menu and select Add Xilinx Device. In the project's implementation directory, select download.bit.



Place cursor over Xilinx chip and right click to select program to download the download.bit file.